

**SECTION I. (AMENDMENTS TO THE CLAIMS)**

A listing of claims 1-21 of the present application, as amended herein with markings to show changes made, is provided below:

1-15. (Cancelled).

16. (Previously presented) A MOSFET device comprising a silicon substrate having shallow trench isolation STI located therein, a gate dielectric and a gate stack located on said silicon substrate, and a fluorine doped low K dielectric oxide gate spacer located on sidewalls of said gate stack, said fluorine doped low K dielectric oxide gate spacer having a fluorine content of about  $1\text{E}14$  to  $2\text{E}16\text{ cm}^{-2}$ .

17. (Previously presented) The MOSFET device of claim 16 wherein said fluorine doped low K dielectric oxide gate spacer has a dielectric constant value in a range of 3.3 to 4.0.

18. (Previously presented) The MOSFET device of claim 16 wherein said fluorine doped low K dielectric oxide gate spacer has a dielectric constant value of substantially 3.3.

19. (Cancelled).

20. (Previously presented) The MOSFET device of claim 16 further comprising a silicon nitride oxide layer located on at least said gate stack.

21. (New) A MOSFET device comprising a silicon substrate having shallow trench isolation STI located therein, a gate dielectric and a gate stack located on said silicon substrate, a fluorine doped low K dielectric oxide gate spacer located on sidewalls of said gate stack, and a silicon nitride oxide layer located on at least said gate stack.